

1. A process for forming an integrated circuit structure having at least one layer of low k material therein and a layer, formed from a low k dielectric layer, suitable for use as an etch stop and/or an etch mask which comprises:

- 5           a) forming a first layer of low k dielectric material over a previously formed integrated circuit structure; and
- b) treating the upper surface of said first layer of low k dielectric material with a plasma to form a first layer of densified dielectric material over the remainder of the underlying first layer of low k dielectric material;

10          whereby said first layer of densified dielectric material is capable of serving as a etch stop and/or an etch mask for etching of said underlying first layer of low k dielectric material.

2. The process of claim 1 including the further step of patterning said first layer of densified dielectric material to form a first etch mask layer of densified dielectric material having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in said underlying first layer of low k dielectric material.

3. The process of claim 2 including the further step of etching said pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer of densified dielectric material thereon.

4. The process of claim 3 wherein said pattern of openings etched in said first layer of low k dielectric material through said first etch mask layer comprises a pattern of trenches extending through said first layer of low k dielectric material down to said previously formed integrated circuit structure.

5. The process of claim 3 wherein said pattern of openings etched in said first layer of low k dielectric material comprises a pattern of vias extending through said first layer of low k dielectric material down to said previously formed integrated circuit structure.

6. The process of claim 1 including the further step of forming a second layer of low k dielectric material over said first layer of densified dielectric material.

7. The process of claim 6 including the further steps of:

- a) forming a protective capping layer of silicon oxide over said second layer of low k dielectric material;
- b) forming over said protective capping layer of silicon oxide a further etch mask having a pattern of openings therein; and
- c) etching a pattern of openings in said capping layer through said further etch mask;
- d) removing said further etch mask; and
- e) etching said second layer of low k dielectric material through said pattern of openings in said protective capping layer, with said first layer of densified material acting as an etch stop.

8. The process of claim 6 including the further step of treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material.

9. The process of claim 8 including the further steps of:

- a) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material; and
- b) etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer, with said first layer of densified dielectric material serving as an etch stop.

10. The process of claim 9, including the further steps of:

- a) forming a pattern of openings in said first etch mask layer through said pattern of openings formed in said second layer of low k dielectric material; and
- b) etching a pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer.

11. The process of claim 10 including the further steps of:

- a) forming another etch mask over said second etch mask layer, said another mask having openings larger than the openings in said pattern of openings in said second etch mask layer; and
- b) etching said larger openings through:
  - i) said second etch mask layer of densified dielectric material; and
  - ii) said second layer of low k dielectric material;

down to said first etch mask layer of densified dielectric material;

10 whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings.

12. The process of claim 6 including the further steps of:

- a) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;
- b) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material;
- c) etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer;
- d) forming a pattern of openings in said first etch mask layer through said pattern of openings formed in said second layer of low k dielectric material; and
- e) etching a pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer.

13. The process of claim 12 including the further steps of:

- a) forming another etch mask over said second etch mask layer, said another etch mask having openings larger than the openings in said pattern of openings in said second etch mask layer; and
- b) etching said larger openings through:
  - i) said second etch mask layer; and
  - ii) said second layer of low k dielectric material;

5 down to said first etch mask layer, using said another etch mask;

whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings.

14. The process of claim 12 wherein said openings formed in said first and second layers of low k dielectric material and said first and second etch mask layers comprise vias, and said process includes the further steps of:

- a) forming a trench mask over said second etch mask layer, said trench mask having openings larger than said vias in said second etch mask layer; and
- b) etching said trenches through:

- i) said second etch mask layer; and
- ii) said second layer of low k dielectric material;

10 down to said first etch mask layer;

whereby said structure will have a pattern of vias formed in said first layer of low k dielectric material and a pattern of trenches formed in said second layer of low k dielectric material, with said trenches in registry with said vias.

15. The process of claim 2 including the further steps of:

- a) forming a second layer of low k dielectric material over said first layer of densified dielectric material;
- b) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material; and
- c) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material;

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17. A process for forming a double damascene structure having a low k material therein which comprises:

- a) forming a first layer of dielectric material over an integrated circuit structure;
- b) forming a first layer of low k dielectric material over said first layer of dielectric material;
- c) treating the upper surface of said first layer of low k dielectric material to form a first layer of densified dielectric material over the remainder of said first layer of low k dielectric material;
- d) forming a second layer of low k dielectric material over said first layer of densified dielectric material;
- e) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;
- f) forming over said second layer of densified dielectric material a via mask having a pattern of via openings therein;
- g) etching via openings in said dielectric layers down to said integrated circuit structure through said via mask;
- h) forming a trench mask over said second layer of densified dielectric material, said trench mask having a pattern of trench openings therein in registry with said via openings; and
- i) etching trenches in said second layer of densified dielectric material and said second layer of low k dielectric material through said trench mask, stopping at said first layer of densified dielectric material.

18. The process of claim 17 wherein said trench mask is removed after forming said pattern of trench openings in said second layer of densified dielectric material and before forming said trenches in said second layer of low k dielectric material; and said trenches are then etched in said second layer of low k dielectric material using said pattern of trench openings already formed in said second layer of densified material as a mask.

19. The process of claim 17 wherein said step of forming a first mask having a pattern of vias  
therein is carried out after said step of treating said upper surface of said first layer of low k  
dielectric material to form a first layer of densified dielectric material over the remainder of  
said first layer of low k dielectric material; said pattern of vias is then etched in said first layer  
5 of densified material through said via mask; said via mask is then removed prior to deposition  
of said second layer of low k dielectric material over said first layer of densified material; and  
said step of etching trenches through said trench mask which trenches stop at said first layer  
of densified material further comprises forming said vias in said first layer of low k dielectric  
material and said first layer of dielectric material through said pattern of via openings  
10 previously formed in said first layer of densified material.

20. A process for forming a double damascene structure having a low k material therein which comprises:

- a) forming a first layer of dielectric material over an integrated circuit structure;
- b) forming a first layer of low k dielectric material over said first layer of dielectric material;
- c) treating the upper surface of said first layer of low k dielectric material to form a first layer of densified dielectric material over the remainder of said first layer of low k dielectric material;
- d) forming over said first layer of densified material a via mask having a pattern of via openings therein;
- e) etching said first layer of densified material through said via mask to replicate in said first layer of densified material said pattern of via openings in said via mask;
- f) removing said via mask;
- g) forming a second layer of low k dielectric material over said first layer of densified dielectric material;
- h) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;
- i) forming over said second layer of densified dielectric material a trench mask having a pattern of trench openings therein in registry with said pattern of via openings in said first layer of densified material;
- j) etching said pattern of trench openings in said second layer of densified dielectric material through said trench mask to replicate in said second layer of densified material said pattern of trenches in said trench mask;
- k) then continuing said trench etch through said second layer of low k dielectric material down to said first layer of densified dielectric material, thereby exposing, at the bottom of said trenches, said pattern of via openings formed in said first layer of densified material; and
- l) then etching vias in said first layer of dielectric material and said first layer of low k dielectric material dielectric layers down to said integrated circuit structure through said exposed pattern of openings previously formed in said first layer of densified material at the bottom of said trenches.

21. The process of claim 20 wherein said trench mask is removed after said step of etching said pattern of trench openings in said second layer of densified material through said trench mask, whereby said pattern of trench openings etched in said second layer of densified material serves as a trench mask for etching said trenches in said second layer of low k material.